A Miniaturized Neuroprosthesis Suitable for Implantation Into the Brain

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***Abstract*—This paper presents current research on a miniaturized neuroprosthesis suitable for implantation into the brain. The prosthesis is a heterogeneous integration of a 100-element microelectromechanical system (MEMS) electrode array, front-end complementary metal–oxide–semiconductor (CMOS) integrated circuit for neural signal preamplification, filtering, multiplexing and analog-to-digital conversion, and a second CMOS integrated circuit for wireless transmission of neural data and conditioning of wireless power. The prosthesis is intended for applications where neural signals are processed and decoded to permit the control of artificial or paralyzed limbs. This research, if successful, will allow implantation of the electronics into the brain, or subcutaneously on the skull, and eliminate all external signal and power wiring. The neuroprosthetic system design has strict size and power constraints with each of the front-end preamplifier channels fitting within the 400 $\times$ 400-μm pitch of the 100-element MEMS electrode array and power dissipation resulting in less than a 1 °C temperature rise for the surrounding brain tissue. We describe the measured performance of initial micropower low-noise CMOS preamplifiers for the neuroprosthetic.**

***Index Terms*—Bio-MEMS, brain, complementary metal–oxide–semiconductor (CMOS) micropower, computer interface, cortical signals, heterogeneous integration, integrated-circuit electronics, low-noise preamplifiers, microelectromechanical system (MEMS) packaging, microelectromechanical system (MEMS) probe, neuroprosthesis, neuroprosthetic devices.**

I. Introduction

PASSIVE microelectrode arrays have been widely used by researchers as a neuroprosthetic tool to extract electrical signals from the brain. The microelectrode arrays are directly connected to measurement instruments through a large bundle of wires and are placed into the brain using surgical techniques. The large number of wires connected to current passive microelectrode arrays limits their widespread use as permanent neuroprosthetic devices. In addition, there is an increasing demand for deploying microelectronics to develop a more sophisticated generation of neuroprosthetic devices capable of producing high-quality electrical signals while significantly reducing the number of connection wires or potentially eliminating the wires entirely using a wireless data link.

A neuroprosthetic implant, such as the one described in this work or reported in [1]–[3], might ultimately control an artificial human prosthesis for paralyzed patients. Such a neuroprosthetic implant would amplify and decode cortical signals in order to control an artificial limb or other external device. Simple visual observation of the performance of the prosthetic system by the patient may close the loop between the artificial prosthesis and the brain.

The development of electronics for the cortical recording is done as a part of a collaborative research program to develop a neuroprosthetic for paralyzed patients [4]. Neurophysiological investigation focuses on cortical recording and evaluation of action planning signals from the posterior parietal cortex (PPC) of monkeys. This area of the cortex may have advantages for applications in neuroprosthetics research. The visual–motor areas of the PPC appear to be very adaptive and able to quickly learn new representations. The parietal reach region (PRR) of the PPC may show little degeneration with paralysis since it provides only modest projections to the spinal cord, and its major afferents appear to be visual, rather than somatosensory. The signals from this region are believed to indicate movement intentions and can provide a source for decoding high-level, cognitive plans for actions. The neurophysiology laboratory has successfully demonstrated real time decoding of neural signals from the PRR. In these closed-loop experiments, monkeys were trained to position a cursor on a computer screen without making an actual reach movement. The cells showed remarkable plasticity in the closed-loop condition, with approximately half of them significantly increasing their direction tuning within 10 to 50 trials when the animals were using the neural activity to position the cursor [5].

II. Heterogeneous Integration of Neuroprosthetic Implant

Heterogeneous integration of commercially available passive Microeelectromechanical system (MEMS)-based electrode arrays with the associated electronic circuitry required the development of bio-MEMS packaging technology. Some specific challenges of this integration include 1) the handling of the MEMS array in a way that allows reliable bonding of the fine

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100-μm joints without damaging the delicate structures and 2) the selection of underfills and coatings capable of isolating the electronics from the body while maintaining biocompatibility. Fig. 1 shows the heterogeneous integration of the neuroprosthetic implant under development, consisting of the MEMS brain probe, integrated complementary metal–oxide–semiconductor (CMOS) electronics and wireless transceiver and power conditioning integrated circuit. The MEMS intracortical electrode array [6] consists of a 10 $\times$ 10 matrix (400μm pitch) of fine, brittle 1-mm-long electrodes. The electrodes are fabricated from Si, which is known to be compatible with brain tissue [7], isolated from one another by rows of SiO_2 and jacketed with SiN. Platinum (Pt) at the tips of the electrodes allows for signal transmission. It should be noted that the chip we have developed can be used with other electrode technologies, such as microwires and tetrodes with simple modification of the connections between the electrode arrays and the chip.

Area array flip-chip technology is used to attach the electronic chip and the MEMS device. The motivations for using flip-chip technology were based on miniaturization to obtain electrical performance improvements and accommodating interconnect density demands. The delicate nature of the Si electrodes complicates the design of the holding fixture. Fragile ledges inhibited the use of mechanical fixtures, and processing temperatures reduced the number of viable adhesives. Through process development, a holding fixture was designed with a cavity that was slightly deeper than the arrays. The fixture incorporated a "shelf" along the edges, which protected the ledges and ensured a relatively even bonding surface. In addition to fixture design and fabrication, the method of array placement within the holding fixtures influenced the quality of the interconnect. Joining processes were investigated using the MEMS electrode arrays and metallized substrates (in place of the electronic chip) [8]. Bonding was performed using both conductive epoxy (FDA approved) and solder. Two heterogeneously integrated neuroprosthetics implants are exhibited in Figs. 1 and 2.

The need for biocompatibility dominated the search for underfills and coatings. However, the fine gap (only 50–75 μm) between the bonded chip and array required the use of a low-viscosity underfill. Once it was proven to completely fill the gap between the electrode array and the substrate without influencing the solder connection, a low-viscosity biocompatible epoxy was chosen as the underfill. After underfilling, the entire assembly was coated with Parylene C because of its low absorption of water and capability to conformally coat, as well as the fact that it has been used in medical implants for some time. It should be noted that the array tips cannot be coated and were thus held in polyethylene glycol (PEG) during the coating procedure. To ensure the function and form of the commercially purchased electrode array as well as that of the fully packaged device, a thorough well-defined incoming/outgoing inspection procedure was developed.

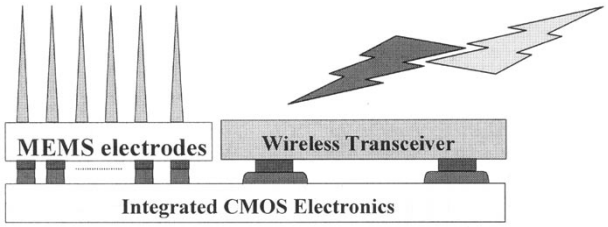

Fig. 1. Heterogeneous integration of neuroprosthetic implant consisting of MEMS probe, integrated front-end CMOS electronics, and wireless transceiver.

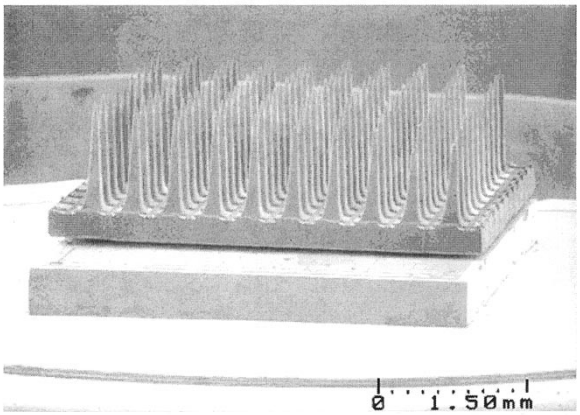

Fig. 2. Scanning electron microscope (SEM) image of a heterogeneously integrated MEMS electrode array and electronic chip.

III. Front-End CMOS Integrated Circuit

Fig. 3 shows a block diagram of the front-end 0.5-μm CMOS integrated circuit under development for neural signal amplification, filtering, multiplexing, dc offset correction, and analog-to-digital (A/D) conversion. An architecture containing an individual preamplifier for each electrode array element was selected to minimize charge injection associated with input multiplexing into a common preamplifier. Charge injection associated with metal–oxide–semiconductor (MOS) transistor switching at the electrode array could significantly disturb adjacent electrode signals as charge is injected back into the brain resistance and capacitance. If charge injection is significantly high, there is also the potential of brain activation.

As shown in Fig. 3, multiplexing will be performed at the output of the front-end preamplifiers, which provides a high degree of charge injection isolation from the multiplexer. Since the preamplifier voltage gains are feedback regulated at typically 80 V/V (the gains are programmable for most of the preamplifiers considered), the presence of MOS device dc mismatch and brain dc offset potentials requires a dc offset subtraction at the multiplexing input circuit. This will be done using a digital-to-analog (D/A) converter to provide the unique correction value for each preamplifier input channel and will be dynamically updated. The dynamic updates from the offset correction circuits eliminate the need for the traditional high-pass filters with very low cutoff frequency for the preamplifiers and enhance the noise performance of the circuit. Following dc offset correction, additional voltage gain will be provided before (A/D) conversion of the conditioned neural signals.

The use of individual electrode array preamplifiers, while minimizing the problems associated with multiplexing charge injection back into the brain, complicates the preamplifier design because of the size constraints associated with 100 pream-

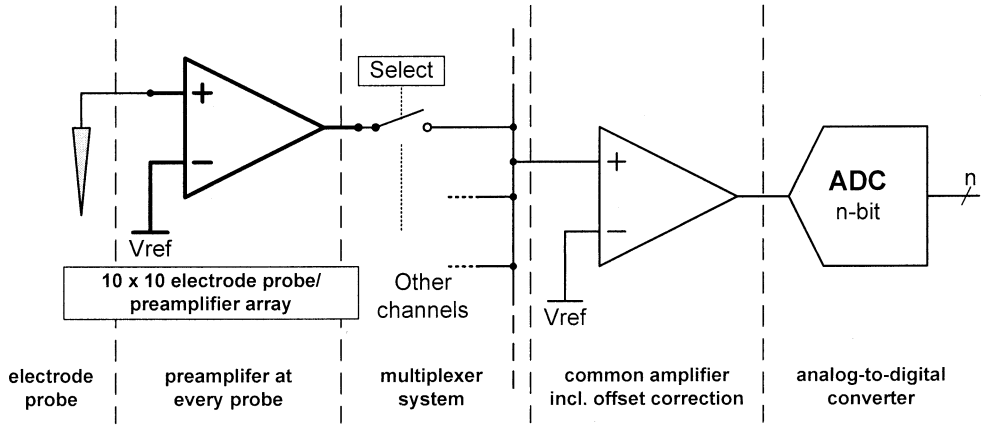

Fig. 3. Block diagram of front-end 0.5-μm CMOS integrated circuit for neural signal amplification, filtering, multiplexing, and analog-to-digital (A/D) conversion.

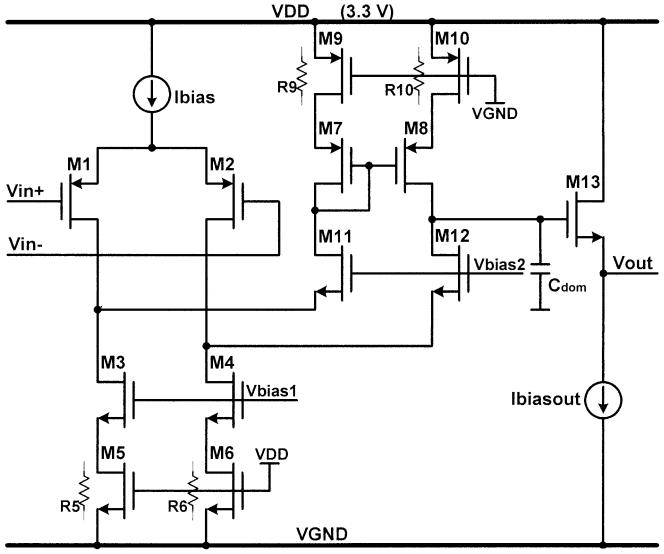

Fig. 4. Abbreviated schematic of micropower low-noise CMOS preamplifier for amplifying each intracortical electrode signal.

plifiers fitted directly behind the 400 $\times$ 400-μm pitch electrode array. In addition, neuroprosthetic implant power consumption must be limited to prevent a brain tissue temperature rise of over 1 °C, which could have long-term effects on the brain. As a result, power efficient micropower low-noise CMOS preamplifiers are critical for the success of this research.

Fig. 4 shows an abbreviated schematic of the micropower, low-noise CMOS preamplifier under development. metal–oxide–semiconductor field-effect transistors (MOSFETs) M1 and M2 comprise a differential pair using large-area p-type metal–oxide–semiconductor (PMOS) devices to minimize low-frequency flicker noise. Signal current from M1 and M2 is routed through the folded cascode configuration of M11 and M12 to the current mirror provided by M7 and M8 that utilizes resistive noise degeneration provided by M9 and M10. High open-loop gain is developed across the compensation capacitor C_{DOM} prior to output voltage buffering provided by source follower M13. M3 and M4 are current sources with resistive noise degeneration provided by M5 and M6. Resistive degeneration is utilized to minimize both white and flicker noise of noninput stages. Considerable attention has been paid to ensuring the input pair devices M1 and M2 dominate both white noise and low frequency flicker noise. Low-frequency flicker noise is of considerable interest because of the low-frequency content of neural signals. Input devices M1 and M2 are operated between weak and moderate inversion to ensure high transconductance efficiency (g_m/I_D) for low input-referred gate noise voltage at the minimum possible bias current. Resistive preamplifier negative feedback, utilizing deep-ohmic PMOS devices, is used for regulating preamplifier voltage gain.

Table I gives the measured noise performance and power dissipation for a 0.35-μm partially depleted silicon-on-insulator (PDSOI) preamplifier used in a proof-of-concept front-end integrated circuit. This integrated circuit contains 64 preamplifiers to support an 8 $\times$ 8-element intracortical electrode array followed by output multiplexing. This integrated circuit will be tested with an intracortical electrode array in laboratory animals to provide guidance on design closure for the final front-end integrated circuit. In addition, Table I illustrates the Simulation Program with Integrated Circuit Emphasis (SPICE) simulated performance of various 0.5-μm bulk CMOS preamplifiers under development, including both a fixed power and a programmable power design. The selection of various power levels is intended to permit the optimum balance of power dissipation and required noise performance. The preamplifier power dissipations given in Table I exclude bias reference circuits that can be common to all 100 preamplifier channels.

IV. Wireless Transceiver and Wireless Power Integrated Circuit

Although an intracortical electrode array and 8 $\times$ 8-element concept front-end integrated circuit have been fabricated for initial evaluations, the wireless transceiver and wireless power integrated circuit is in the early concept stages. Key issues here will be transmitting digital neural information at the required

TABLE I
INTRACORTICAL ELECTRODE ARRAY CMOS PREAMPLIFIER PERFORMANCE

CMOS process	Power per channel	Total input noise[a]	Input noise at 1 Hz	Input white noise floor	1/f corner frequency	Notes
0.35-μm, PDSOI CMOS	9.9 μW at 3.3 V	8.2 μVrms (measured)	300 nV/√Hz (measured)	65 nV/√Hz (measured)	8 Hz (measured)	1 μA pair current, A_V = 49 V/V, fixed power
0.5-μm bulk CMOS	60 μW at 5 V	3.9 μVrms	170 nV/√Hz	30 nV/√Hz	45 Hz	4 μA pair current, A_V = 81 V/V, fixed power
	15 μW at 5 V	8.7 μVrms	185 nV/√Hz	67 nV/√Hz	10 Hz	1 μA pair current, A_V = 81 V/V, prog. power
	60 μW at 5 V	4.5 μVrms	171 nV/√Hz	33 nV/√Hz	33 Hz	4 μA pair current, A_V = 81 V/V, prog. power
	240 μW at 5 V	2.5 μVrms	160 nV/√Hz	17 nV/√Hz	100 Hz	16 μA pair current, A_V = 81 V/V, prog. power

[a] Noise integrated over a bandwidth of 1 Hz to 10 kHz.

rate and minimizing coupled energy associated with wireless transmission of power while ensuring less than a 1 °C temperature rise in neighboring brain tissue.

V. CONCLUSION

Current research on a neuroprosthetic implant containing a 100-element MEMS electrode array integrated with CMOS electronics has been presented here. The prosthesis is intended for applications where neural signals are processed and decoded to permit the control of artificial or paralyzed limbs. Flip-chip technology was chosen for the integration of the electronics and MEMS electrode array to accommodate the high density of interconnections. The underfills and coatings chosen for the flip-chip design as well as the Si-fabricated electrodes are biocompatible with brain tissue. An array of CMOS preamplifiers was designed and evaluated for neural signal preamplification at micropower levels necessary to ensure less than 1 °C temperature rise in surrounding brain tissue. Research is ongoing for filtering, multiplexing, and data conversion of neural signals with wireless transmission to eliminate all external wiring.

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